

Title of the Invention

COLD CATHODE TYPE FLAT PANEL DISPLAY

Background of the Invention and Related Art

5       The present invention relates to a cold cathode type flat panel display, in particular, a spontaneously emitting type flat panel display using cold cathode electron sources.

10      As known well, a cold cathode type flat panel display is a display that comprises a phosphor film which is formed on a flat panel and emits by electron excitation and very small cold cathode electron sources arranged in a two-dimensional matrix form so as to be opposed to the phosphor film, and that has a function 15     of irradiating the phosphor film with electron rays emitted from the electron sources to display an image on the panel. Displays using such very small cold cathode electron sources which can be integrated are generically named field emission displays (FEDs).

20      Cold cathode electron sources are roughly classified to field emission type electron sources and hot electron type electron sources. Examples of the former include a spindt type electron source, a surface conduction type electron source, and a carbon nano-tube 25     type electron source. Examples of the latter include a metal-insulator-metal (MIM) type electron source, wherein a metal, an insulator and a metal are laminated, and a metal-insulator-semiconductor (MIS) type electron

source, wherein a metal, an insulator and a semiconductor are laminated.

The MIM type electron source is disclosed in, for example, Japanese Patent Application Laid-Open No.

5 2001-101965 (Patent Document 1) and Japanese Patent Application Laid-Open 2000-208076 (Patent Document 2). A structure of the MIM electron source and the operation principle thereof are shown in FIGS. 1 and 2.

FIG. 1 is a sectional structural view of an MIM type electron emitting element. In FIG. 1, bottom electrodes 11, made of, e.g., Al or Al alloy, are formed on an insulating cathode substrate 10 made of glass or the like so as to have a thickness of, e.g., 300 nm and be in a stripe form in the direction perpendicular to the surface of the drawing paper.

An interlayer insulator 14 (film thickness: e.g., 140 nm) for preventing the concentration of an electric field at edges of the bottom electrodes 11 and limiting or laying down an electron emission area, and 20 a tunneling insulator 12 (film thickness: e.g., 10 nm) are formed.

Contact electrodes 15 and top electrode bus lines 16 are formed in a stripe form in the direction perpendicular to the bottom electrodes 11 (i.e., the 25 right and left direction in the drawing paper), so as to avoid the electron emission area E. The electron emission area E corresponds to top electrodes 13 on the tunneling insulator 12. The top electrodes will be

described in detail later.

The contact electrodes 15 are made of a metal film having a strong adhesive force to the cathode substrate 10 or the interlayer insulator 14, for example, a high melting point metal such as W (tungsten) or Mo (molybdenum) or a silicon compound thereof (silicide), so as to have a film thickness of, e.g., about 10 nm.

The top electrode bus lines 16 are bus lines which can be connected to the top electrodes 13, which will be detailed later, at a low resistance and are made of an Al-Nd alloy film, so as to have a thickness of 200 nm. In order to prevent the snapping of the top electrodes 13, which will be detailed later, it is desired that a metal film as thin as possible. for the contact electrodes is made as thin as possible.

On the top electrode bus lines 16, the interlayer insulator 14 and the cathode substrate 10 except the electron emission area E, a surface protection film 17 is formed, which is an insulator film made of, for example, intrinsic silicone, SiO<sub>2</sub>, glass (such as phosphor doped glass or boron doped glass), Si<sub>3</sub>N<sub>4</sub> (nitride), Al<sub>2</sub>O<sub>3</sub> (alumina) or polyimide. For reference, in the case of using Si<sub>3</sub>N<sub>4</sub>, the film thickness thereof is from 0.1 to 1 μm.

The tunneling insulator 12 is covered with top electrodes 13. The top electrodes 13 have a three-layer structure composed of a lower layer made of Ir

(iridium), which is good in heat resistance, an intermediate layer made of Pt (platinum) and an upper layer made of Au (gold), which is good in electron emitting efficiency, and are applied onto the tunneling insulator 12 in a thin film forming step using, for example, sputtering.

In this thin film forming step, the layer of the top electrodes 13 is simultaneously deposited on the surface of the surface protection film 17. As shown in FIG. 1, however, the layer of the top electrode bus lines 16 retreats inwards from end faces of the surface protection film 17 so that the surface protection film 17 is made into the form of eaves. Consequently, a metal film 13' on the surface protection film 17 is electrically insulated from the top electrodes 13 on the tunneling insulator 12.

When a voltage  $V_d$  is applied between the bottom electrodes 11 and the top electrodes 13 of the MIM type electron emitting element having a structure as described above in vacuum, electrons, in the bottom electrodes 11, having an energy level near the Fermi level penetrate through a potential barrier by tunneling phenomena, so as to be injected into the conduction band of the tunneling insulator 12 and the top electrodes 13. As a result, hot electrons are generated. Among these electrons, electron having a kinetic energy equal to or more than the work function  $\phi$  of the top electrodes 13 are emitted into the vacuum.

A document related to such a technique is  
Japanese Patent Application Laid-Open No. 2001-83907  
(Patent Document 3).

FIG. 46 is a sectional view illustrating an  
outline of a display panel in the prior art. As  
illustrated in this figure, in order to use the above-  
mentioned MIM type electron sources to construct a  
display device, the cathode electrode 10 wherein the  
electron sources having the structure illustrated in  
FIG. 1 are arranged in a matrix form and an anode  
substrate 110 wherein phosphor film pieces 111 are  
arranged in a matrix form so as to correspond to the  
electron source elements of the cathode substrate 10  
are adhered through a glass frame member 116 made of  
glass or the like by junction based on frit glass 115,  
thereby making an inner space 118 into vacuum. In this  
way, a display panel (flat panel display) 120 is  
yielded. As will be described in more detail later,  
the anode substrate 110 is made of a light-transmitting  
flat panel, and the whole of a single surface of the  
anode substrate 110, including the surfaces of the  
phosphor film pieces 111, is covered with a conductive  
film (called a metal back) 114.

When the diagonal size of the display panel 120  
is more than 5 inches in this case, it is necessary to  
insert spacers 30 made of an insulator material, as  
reinforcing materials, at intervals of several  
centimeters into the inner space (vacuum atmosphere) of

the panel in order to keep the atmospheric pressure.

A part of electrons emitted from the electron source elements collides with these spacers 30, so that the spacers 30 are charged up. Near the charged  
5 spacers, the orbit of the electrons is curved so as to cause a phenomenon that an image is distorted. In order to prevent this phenomenon, a slight conductivity is given to the surface of the spacers 30 by means of a high-resistance film made of tin oxide, a mixed crystal  
10 thin film made of tin oxide and indium oxide, a metal film, a semiconductor film or some other film. In this way, the electrification of the spacer surfaces is removed.

It is therefore necessary to connect the  
15 spacers 30 electrically to the metal back 114 on the side of the anode substrate 110 and the top electrodes 13' on the surface protection film 17 on the side of the cathode substrate 10. The top electrodes 13' for giving grounding voltage on the side of the cathode  
20 substrate 10 have a thickness of 10 nm or less and further have a weak adhesive force to the surface protection film 17; therefore, when pressure from the spacers is applied to the top electrodes 13', the snapping or breaking down thereof is easily caused. In  
25 order to prevent this, it is necessary to set third bus lines independently of the data lines (the top electrode bus lines 16 and the scan lines (the bottom electrodes 11), as ground lines 18 for the spacers 30,

on the surface protection film 17.

However, in the case of adopting the three-layer line structure wherein the data lines 16, the scan lines 11 and the third bus lines independently thereof are set on the side of the cathode substrate 10 as described above, the production process thereof unavoidably becomes longer than the production process including the formation of two-layer bus lines. As a result, problems of a drop in the yield or an increase in the production costs are caused.

#### Objects and Summary of the Invention

Accordingly, an object of the present invention is to solve the above-mentioned problems and provide a cold cathode type flat panel display (specifically, a hot electron type cold cathode type flat panel display) comprising a cathode substrate which has a two-layer structure but substantially has ground lines for spacers which can be inexpensively produced.

As a result of various experiments and examinations, the inventors have obtained the finding that the above-mentioned problems can be solved by taking the following measurements: a cathode substrate which has a two-layer line structure but substantially has ground lines, for spacers, having a stable structure can be realized by contriving its line structure as follows:

(1) Hitherto, bottom electrodes, which are first layer

(lower layer) lines used as scan lines, are made into data lines (conventional scan lines are converted to data lines), and

5 (2) Spacer lines and scan lines made of second layer lines (top electrode bus lines) are formed so as to display an image according to a line sequential scanning scheme (conventional data lines are converted to scan lines).

10 First, by the item (1), the scan data and the spacer lines can be extended in the same direction. In addition, the second lines are used to make the scan lines and the spacer lines from the same layer.

15 Questions may be put up to the practicability of the above-mentioned line structure. However, the present invention has a sufficient basis.

20 In general, the shape of each of pixels is a square. A scan line pitch corresponds to the length of each side of this square. The pitch of data lines is 1/3 of the length since each of the pixels includes three colors, that is, red (R), green (G) and blue (B). Specifically, for example, in a WXGA (resolution: 720 × 1200 dots) having a diagonal size of 32 inches, the scan data pitch thereof and the data line pitch thereof are 550  $\mu$ m and 183  $\mu$ m, respectively.

25 Since the thickness of ordinary spacers themselves is from about 100 to 200  $\mu$ m, it can be said that the structure of the present invention, wherein spacers and ground lines for the spacers are inserted

between scan lines having a wide pitch, is a reasonable design.

When the above is summarized, the following conclusion can be obtained: by adopting the present invention, lines composed of three layers in the conventional cathode substrate 10 are unified into lines composed of two layers; accordingly, the interlayer insulator present between the third lines and the second lines in the cathode substrate 10 becomes unnecessary.

As described above, according to the present invention, the line structure of its cathode substrate is changed from the three-layer line structure in the prior art to a two-layer line structure and further ground lines for its spacers are formed, as the same layer as is made up to top electrode bus lines which constitute scan lines, on the same flat surface. Therefore, the line structure is simple and further the top electrode bus lines and the ground lines for the spacers can be produced in the same step. As a result, the production process of the display of the present invention can be shortened and an improvement in the yield thereof and a drop in the production costs thereof can be attained.

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#### Brief Description of the Drawings

FIG. 1 is a view illustrating an MIM type electron source in the prior art.

FIG. 2 is a view illustrating the operation principle of the MIM type electron source.

FIG. 3 is a plan view illustrating the step of forming a bottom electrode 11 in the production of an  
5 MIM type electron source of the present invention.

FIG. 4 is a sectional view of the members illustrated in FIG. 3, taken on line A-A', in the production of the MIM type electron source of the present invention.

10 FIG. 5 is a sectional view of the members illustrated in FIG. 3, taken on line B-B', in the production of the MIM type electron source of the present invention.

15 FIG. 6 is a plan view illustrating the step of forming a tunneling insulator 12 on the bottom electrode 11 in the production of the MIM type electron source of the present invention.

20 FIG. 7 is a sectional view of the members illustrated in FIG. 6, taken on line A-A', in the production of the MIM type electron source of the present invention.

25 FIG. 8 is a sectional view of the members illustrated in FIG. 6, taken on line B-B', in the production of the MIM type electron source of the present invention.

FIG. 9 is a plan view illustrating the step of forming contact electrodes 15A and 15B in the production of the MIM type electron source of the

present invention.

FIG. 10 is a sectional view of the members illustrated in FIG. 9, taken on line A-A', in the production of the MIM type electron source of the present invention.

FIG. 11 is a sectional view of the members illustrated in FIG. 9, taken on line B-B', in the production of the MIM type electron source of the present invention.

FIG. 12 is a plan view illustrating the step of forming top electrode bus lines 16 and spacer lines 16' in the production of the MIM type electron source of the present invention.

FIG. 13 is a sectional view of the members in FIG. 12, taken on line A-A', in the production of the MIM type electron source of the present invention.

FIG. 14 is a sectional view of the members in FIG. 12, taken on line B-B', in the production of the MIM type electron source of the present invention.

FIG. 15 is a plan view illustrating the step of producing the MIM type electron source of the present invention.

FIG. 16 is a sectional view of the members illustrated in FIG. 15, taken on line A-A', in the step of producing the MIM type electron source of the present invention.

FIG. 17 is a sectional view of the members illustrated in FIG. 15, taken on line B-B', in the step

of producing the MIM type electron source of the present invention.

FIG. 18 is a plan view illustrating the step of producing the MIM type electron source of the present invention.

FIG. 19 is a sectional view of the members illustrated in FIG. 18, taken on line A-A', in the step of producing the MIM type electron source of the present invention.

FIG. 20 is a sectional view of the members illustrated in FIG. 18, taken on line B-B', in the step of producing the MIM type electron source of the present invention.

FIG. 21 is a plan view illustrating the step of producing the MIM type electron source of the present invention.

FIG. 22 is a sectional view of the members illustrated in FIG. 21, taken on line A-A', in the step of producing the MIM type electron source of the present invention.

FIG. 23 is a sectional view of the members illustrated in FIG. 21, taken on line B-B', in the step of producing the MIM type electron source of the present invention.

FIG. 24 is a plan view of a cathode substrate 10 of the present invention.

FIG. 25 is a sectional view of the cathode substrate 10 of the present invention, taken on line A-

A' of FIG. 24.

FIG. 26 is a sectional view of the cathode substrate 10 of the present invention, taken on line B-B' of FIG. 24.

5 FIG. 27 is a plan view illustrating the production process of an anode substrate 110 using MIM type electron sources of the present invention.

10 FIG. 28 is a sectional view illustrating the production process of the anode substrate 110 using the MIM type electron sources of the present invention, taken on line A-A' of FIG. 24.

15 FIG. 29 is a sectional view illustrating the production process of the anode substrate 110 using the MIM type electron sources of the present invention, taken on line B-B' of FIG. 24.

20 FIG. 30 is a sectional view illustrating the production process of a display device using the MIM type electron sources of the present invention, taken on line A-A' similar to the line in the cathode substrate 10.

25 FIG. 31 is a sectional view illustrating the production process of a display device using the MIM type electron sources of the present invention, taken on line B-B' similar to the line in the cathode substrate 10.

FIG. 32 is a plan view of a display device schematically illustrating the state of line-connection between a display panel 120 of the present invention

and driver circuits.

FIG. 33 is a diagram showing driving voltage waveforms in the display device of the present invention.

5 FIG. 34 is a plan view of a display device schematically illustrating the state of line-connection between a display panel 120 of the present invention and driver circuits.

10 FIG. 35 is a plan view of a display device schematically illustrating the state of line-connection between the display panel 120 of the present invention and driver circuits.

15 FIG. 36 is a plan view illustrating a different production process of the MIM type electron sources of the present invention.

FIG. 37 is a sectional view illustrating the different production process of the MIM type electron sources of the present invention, taken on line A-A' of FIG. 36.

20 FIG. 38 is a sectional view illustrating the different production process of the MIM type electron sources of the present invention, taken on line B-B' of FIG. 36.

25 FIG. 39 is a plan view illustrating the production process of the cathode substrate 10, which is the different example of the present invention.

FIG. 40 is a sectional view illustrating the different example of the MIM type electron sources of

the present invention, taken on line A-A' of FIG. 39.

FIG. 41 is a sectional view illustrating the different example of the MIM type electron sources of the present invention, taken on line B-B' of FIG. 39.

5 FIG. 42 is a sectional view illustrating the production process of the display device, which is the different example using the MIM type electron sources of the present invention, taken on line A-A'.

10 FIG. 43 is a sectional view illustrating the production process of the display device, which is the different example using the MIM type electron sources of the present invention, taken on line B-B'.

15 FIG. 44 is a plan view of a display device schematically illustrating the state of line-connection between the display panel 120, which is the different example of the present invention, and driver circuits.

FIG. 45 is a diagram illustrating driving voltage waveforms in the display device which is the different example of the present invention.

20 FIG. 46 is a sectional viewing illustrating a display panel using an MIM type electron source in order to describe the prior art.

Reference numbers in the above-mentioned drawings are as follows.

25 10: cathode substrate, 11: bottom electrode (data line),  
12: tunneling insulator, 13 and 13': top electrode, 14:  
interlayer insulator, 15: contact electrode, 16: top  
electrode bus line (scan line), 16': spacer line, 17:

surface protection film, 18: spacer ground line, 20:  
vacuum level, 30: spacer, 40: data line driver circuit,  
50: scan line driver circuit, 60: high voltage  
generating circuit, 70: flexible printed circuit (FPC),  
5 110: anode substrate, 111: red phosphor, 112: green  
phosphor, 113: blue phosphor, 114: metal back, 115:  
frit glass, 115': conductive frit glass, 116: glass  
frame, 117: black matrix, 118: vacuum, 120: display  
panel, E: electron emission area, and e: emitted  
10 electron.

#### Detailed Description of Preferred Embodiments

A first aspect of the present invention is  
typically a cold cathode type flat panel display which  
15 is an image display device comprising a vacuum panel  
container composed of a cathode substrate in which  
plural cold cathode type electron sources are arranged  
at regular intervals, an anode substrate in which a  
phosphor film is deposited in the form of dots or lines  
20 so as to be opposed to the electron sources, plural  
spacers for supporting the cathode substrate and the  
anode substrate at a given interval, and a glass frame.

Plural electrical lines which extend in a line  
direction and a row direction which cross each other  
25 are formed, across an interlayer insulator, on the  
cathode substrate; the cold cathode type electron  
sources are arranged at positions corresponding to  
intersection coordinates of these electrical lines so

as to be connected to the electrical lines in the line direction and the row direction; and the cold cathode type electron sources are line-sequentially scanned, thereby displaying images.

5           In this image display device, some parts of lines positioned in the upper layer out of the plural electrical lines are made into scan lines and lines positioned in the lower layer out of the plural electrical lines are made into data lines, and

10          some parts of the electrical lines positioned in the upper layer are made into ground lines for giving ground voltage to the spacers, and further the spacers are in a ground state by the ground lines at the least in the period when the scan lines adjacent thereto are selected.

15          A second aspect of the present invention is typically a cold cathode type flat panel display which is an image display device comprising a vacuum panel container composed of a cathode substrate in which plural cold cathode type electron sources are arranged at regular intervals, an anode substrate in which a phosphor film is deposited in the form of dots or lines so as to be opposed to the electron sources, plural spacers for supporting the cathode substrate and the anode substrate at a given interval, and a glass frame.

20          Plural electrical lines which extend in a line direction and a row direction which cross each other are formed, across an interlayer insulator, on the

cathode substrate; the cold cathode type electron sources are arranged at positions corresponding to intersection coordinates of these electrical lines so as to be connected to the electrical lines in the line 5 direction and the row direction; and the cold cathode type electron sources are line-sequentially scanned, thereby displaying images.

In this image display device, lines positioned in the upper layer out of the plural electrical lines 10 are made into scan lines and lines positioned in the lower layer out of the plural electrical lines are made into data lines, and

some parts of the scan lines positioned in the upper layer function both as power feeding lines for 15 giving electric potential to the spacers and scan lines, and are at scan line voltage at the least in the period when the parts of the scan lines are selected.

A third aspect of the present invention is as follows: in the cold cathode type flat panel display 20 according to the first or second aspect, in an edge portion of the cathode substrate, terminals of the electrical lines positioned in the upper layer are connected to a flexible printed circuit (abbreviated to FPC) connected to a scan line driver circuit, and 25 supply electric potential to the spacer lines through the scan line driver circuit.

A fourth aspect of the present invention is as follows: in the cold cathode type flat panel display

according to the first aspect, in an edge portion of  
the cathode substrate, terminals of the electrical  
lines positioned in the upper layer are connected to a  
flexible printed circuit connected to a scan line  
5 driver circuit, and supply ground voltage from the  
outside through independent power feeding lines in the  
state that the spacer lines are mutually short-  
circuited through internal lines of the flexible  
printed circuit.

10 A fifth aspect of the present invention is as  
follows: in the cold cathode type flat panel display  
according to the first aspect, the spacer lines in the  
edge portion of the cathode substrate are extended to  
the outside of terminals of the scan lines and are  
15 mutually short-circuited, and the spacer lines give  
ground voltage from the outside through independent  
power feeding lines.

A sixth aspect of the present invention is as  
follows: in the cold cathode type flat panel display  
20 according to any one of the first to fifth aspects, the  
cold cathode type electron sources each have a  
structure wherein a bottom electrode, an electron  
accelerator, and a top electrode are laminated in this  
order, and are each an electron source element which  
25 emits electrons from the surface of the top electrode  
when a positive voltage is applied to the top electrode.

A seventh aspect of the present invention is as  
follows: in the cold cathode type flat panel display

according to the sixth aspect, the bottom electrode of each of the cold cathode type electron sources is made of Al or Al alloy, and the electron accelerator is made of alumina obtained by subjecting the Al or Al alloy to  
5 anodic oxidation.

#### Examples

An example of the present invention will be specifically described with reference to the attached  
10 drawings hereinafter.

##### Example 1

An example according to the first aspect of the present invention will be described with reference to FIGS. 3 to 33.

###### 15 (1) Formation of a cathode substrate 10:

This item describes a production process in a case in which top electrodes 13 are connected electrically to contact electrodes 15 and further top electrode bus lines 16 are backed with aluminum,  
20 aluminum alloy, or a metal having a lower resistivity than aluminum.

It is beforehand stated that the MIM electron source producing process which can be used in the present invention is not limited to the present example.

25 The present invention can easily be applied to MIM electron sources disclosed in Patent Documents 1 and 2 (Japanese Patent Application Laid-Open Nos. 2001-101965 and 2000-208076), which comprise top electrode bus

lines having a tapered structure, and other MIM electron sources.

First, a metal film for bottom electrodes 11 is deposited on an insulating cathode substrate 10 made of  
5 glass or the like. As the material for the bottom electrode, Al or Al alloy is used. Actually, Al-Nd doped with 2% by atom of Nd was used. For the formation of the metal film, for example, sputtering is used. Actually, the film thickness thereof was set to  
10 300 nm. After the formation of the metal film, the bottom electrodes 11, in a stripe form as illustrated in FIG. 3 (a plan view), FIG. 4 (a sectional view taken on line A-A'), and FIG. 5 (a sectional view taken on line B-B') are formed through a photolithographic step  
15 and an etching step. In the etching step, there is used, for example, wet etching based on an aqueous mixed solution of phosphoric acid, acetic acid and nitric acid.

As illustrated in FIG. 6 (a plan view), FIG. 7  
20 (a sectional view taken on line A-A'), and FIG. 8 (a sectional view taken on line B-B'), the surfaces of the bottom electrodes 11 are subjected to anodic oxidation. For example, when the formation voltage is set to 6V, an insulator layer 12 having a thickness of about 10 nm  
25 is formed on the bottom electrodes 11.

As illustrated in FIG. 9 (a plan view), FIG. 10 (a sectional view taken on line A-A'), and FIG. 11 (a sectional view taken on line B-B'), Si<sub>3</sub>N<sub>4</sub> for an

interlayer insulator 14, Cu for an upper contact electrode layer 15B, which will be a seed film for plating, and Cr for a lower contact electrode layer 15A for ensuring adhesiveness between Cu and the underlying thereof are continuously deposited by sputtering. The lower contact electrode layer 15A is made as thin as about several ten nanometers in such a manner that the snapping of top electrodes 13, which will be formed later, will not be caused by difference in level in the lower contact electrode layer 15A. The film thickness of the upper contact electrode layer 15B is not particularly limited. However, the film thickness is set in such a manner that the lower contact electrode layer 15A will not elute out at the time of plating treatment.

As illustrated in FIG. 12 (a plan view), FIG. 13 (a sectional view taken on line A-A'), and FIG. 14 (a sectional view taken on line B-B'), resist patterns as plating masks are given to the upper contact electrode layer 15B, and subsequently Cu is thickly deposited by electroplating or electroless plating, so as to form top electrode bus lines 16 made of Cu and having a thickness of, e.g., 5 im (in the figures, the lines 16 are drawn in the state that the thickness thereof is scaled down for appearance' sake).

Any one of these figures illustrates the state after the thickly plating of Cu is completed and then the plating masks (resist patterns) are removed. The

resist patterns are of two kinds, one of which is a square pattern for forming an electron emission area for electron sources, and the other of which is a stripe-form pattern for dividing areas which will be  
5 the top electrode bus lines 16 and spacer lines 16'.

As illustrated in FIG. 15 (a plan view), FIG. 16 (a sectional view taken on line A-A'), and FIG. 17 (a sectional view taken on line B-B'), Cu in the entire surface is etched to work the thin upper contact  
10 electrode layer 15B into a stripe form in the direction perpendicular to the bottom electrodes 11. Since the upper contact electrode layer 15B is far thinner than the top electrode bus lines 16, only the upper contact electrode layer 15B can be selectively removed by  
15 controlling the time for the etching. As the etchant, for example, an aqueous mixed solution of phosphoric acid, acetic acid and nitric acid (PAN) is suitable.

Subsequently, a resist pattern in the form of a square frame is formed on the lower contact electrode  
20 layer 15A for forming the electron emission area (square concave portion) for electron sources. The lower contact electrode layer 15A (Cr) naked inside the frame-form pattern is selectively worked by wet etching, so as to be removed. For the wet etching of Cr, an  
25 aqueous solution of cerium diammonium nitrate is suitable. Attention should be paid to the matter that the frame-form resist pattern is formed to cover the peripheral end of the lower contact electrode layer 15A,

as described above. In this way, top electrodes 13, which will be formed later, will overlap with the lower contact electrode layer 15A without breaking off so as to be connected to the layer 15A.

5 As illustrated in FIG. 18 (a plan view), FIG. 19 (a sectional view taken on line A-A'), and FIG. 20 (a sectional view taken on line B-B'), a hole is made in a part of the interlayer insulator 14 by photolithography and dry etching in order to open the 10 electron emission area in the concave portion which will make the electron emission area for electron sources. In this way, a tunneling insulator 12 is made naked. For the etching gas, a mixed gas of CF<sub>4</sub> and O<sub>2</sub> is suitable. The naked tunneling insulator 12 is again 15 subjected to anodic oxidation to repair work-damage based on the etching.

As illustrated in FIG. 21 (a plan view), FIG. 22 (a sectional view taken on line A-A'), and FIG. 23 (a sectional view taken on line B-B'), top electrodes 20 13 are formed to complete an electron source substrate (finished cathode substrate 10). The formation of the film for the top electrodes 13 is performed by sputtering using a shadow mask. In this way, the top electrode bus lines 16 are separated from each other.

25 As the material for the top electrodes 13, the above-mentioned laminated films of Ir, Pt and Au are used. The film thickness of each of the films is set to several nanometers. This makes it possible to avoid

damage to the top electrodes or the tunneling insulator, associated with the photolithography and etching.

The following will describe a process for producing the whole of a display device, using the MIM type electron source substrate (finished cathode substrate 10).

First, a cathode substrate wherein plural MIM type electron sources are arranged on the cathode substrate 10 is formed in accordance with the above-mentioned production process.

To simplify the description hereinafter, a plan view and sectional views of the cathode substrate 10 which is a  $3 \times 4$  dot MIM type electron source substrate are shown in FIG. 24 (a plan view), FIG. 25 (a sectional view taken on line A-A'), and FIG. 26 (a sectional view taken on line B-B'). Actually, an MIM type electron source matrix wherein the number of MIM type electron sources corresponds to the number of display dots should be formed.

In the case that a display device is constructed, electrode ends of the bottom electrodes 11 and the top electrode bus lines 16 must be made naked in order to connect the ends to driver circuits although this matter has not been referred to, in the description on the process for producing the MIM type electron source, hereinbefore.

(2) Formation of an anode substrate 110:

Referring to FIG. 27 (a plan view), FIG. 28 (a

sectional view taken on line A-A'), and FIG. 29 (a sectional view taken on line B-B'), a process for producing an anode substrate 110 will be described.

As the anode substrate 110, light-transmitting  
5 glass is used. First, a black matrix 117 is formed in order to raise the contrast of the display device to be produced. The black matrix 117 is formed by applying a solution wherein polyvinyl alcohol (PVA) and ammonium chromate are mixed to the anode substrate 110,  
10 irradiating the portion other than the portion where the black matrix 117 is to be formed with ultra-violet rays so as to be sensitized, removing the non-sensitized portion, applying a solution where graphite powder is dissolved thereto, and then lifting off PVA.

15 Next, a red phosphor 111 is formed. An aqueous solution wherein phosphor particles are mixed with PVA and ammonium chromate is applied onto the anode substrate 110, and then the portion where the phosphor is to be formed is irradiated with ultra-violet rays so  
20 as to be sensitized, and then the non-sensitized portion is removed with flowing water. In this way, the red phosphor 111 is patterned.

The pattern is made into a dot-form pattern as illustrated in FIGS. 27, 28 and 29. In the same way, a  
25 green phosphor 112 and a blue phosphor 113 are formed. About the phosphors, it is advisable to use  $\text{Y}_2\text{O}_2\text{S}:\text{Eu}$  (P22-R) for the red,  $\text{ZnS}:\text{Cu}$  or  $\text{Al}$  (P22-G) for the green, and  $\text{ZnS}:\text{Ag}$  (P22-B) for the blue.

Next, the resultant is filmed with a film made of nitrocellulose or the like, and subsequently Al is vapor-deposited on the anode substrate 110 so as to have a thickness of about 75 nm, thereby forming a metal back 114. This metal back 114 functions as an accelerating electrode. Thereafter, the anode substrate 110 is heated to about 400 °C in the atmosphere to heat-decompose organic substances, such as the filming film or PVA. In this way, a finished anode substrate 110 is yielded.

10 (3) Formation of a display panel:

The finished anode substrate 110 and the finished cathode substrate 10, formed as described above, are adhered to a surrounding glass frame 116 through spacers 30 with frit glass 115.

FIG. 30 illustrates a section of a display panel 120 obtained by the adhesion, this section corresponding to the section taken on line A-A', and FIG. 31 illustrates a section of the display panel 120, this section corresponding to the section taken on line B-B'. The section taken on line A-A' and the section taken on line B-B' of the display panel correspond to line A-A' and line B-B' in cases where the cathode substrate 10 and the anode substrate 110 are drawn, respectively.

25 The height of the spacers 30 is set in such a manner that the distance between the anode substrate 110 and the cathode substrate 10 will be from about 1

to 3 mm. The spacers 30 are made of glass or ceramic in the form of a plate. Electrical conductivity is given at least to the surface of the glass or ceramic. One-side ends of the spacer 30 are arranged on the 5 spacer lines 16' adjacent to the top electrode bus lines 16, and they are electrically connected to each other.

The other-side ends of the spacers 30 are arranged beneath the black matrix 117 on the display 10 substrate side (the side of the anode substrate 110), and are fixed with an adhesive material such as conductive frit glass 115'. Therefore, the spacers 30 do not hinder light emission from the phosphors. Electrical connection between each of the spacer 30 and 15 the corresponding spacer line 16' is attained by inserting the spacer 30 between the cathode substrate 10 and the anode substrate 110 under pressure and then bringing one end thereof into contact with the spacer line 16', or may be attained by a conductive paste if 20 necessary.

In the case that the spacers 30 are members obtained by coating an insulator such as glass or ceramic with a conductive material having electron conductivity as described above so as to set the sheet 25 resistance to 1E+10 to 1E+13 Ω/square, or are conductive glass or ceramic obtained by giving electrical conductivity to such an insulator itself, the spacers 30 are preferably spacers having electron

conductivity and a volume resistance of, e.g.,  $1E+8$  to  $1E+11 \Omega\cdot\text{cm}$ .

As illustrated in FIG. 31, in this example, the spacers 30 are caused to stand on the respective  
5 phosphor dots which emit red (R), green (G) and blue (B), that is, all of the spacer lines 16'. However, in actual display panels, the number (density) of the spacers 30 may be decreased within such a scope that necessary mechanical strength can be obtained. Roughly,  
10 the spacers 30 may be caused to stand at intervals of several centimeters.

Instead of the plate-form spacers 30, pillar type spacers or cross type spacers may be used in other examples. In such a case, a panel can be fabricated in  
15 the same or similar way.

The panel 120 the peripheral edge portion of which is sealed is degassed into a vacuum of  $10^{-7}$  Torr in pressure so as to be sufficiently sealed up. After the sealing, a getter inside the panel is activated and  
20 the inside of the panel is kept in a high vacuum. For example, in the case of a getter material made mainly of Ba, a getter film can be formed by high frequency heating or the like. A non-evaporating type getter made mainly of Zr may be used. In this way, the  
25 finished display panel 120 using the MIM type electron sources is yielded.

As described above, in the present example, the distance between the anode substrate 110 and the

cathode substrate 10 is as long as about 1 to 3 mm. Accordingly, the acceleration voltage applied to the metal back 114 can be made as high as 1 to 10 kV, thereby making it possible to use, as the phosphors,  
5 phosphors for a cathode ray tube.

FIG. 32 is a connection diagram wherein the display device panel 120 produced as described above is connected to driver circuits, and illustrates an outline of the whole of an electric circuit for driving  
10 the display device of the present example.

The bottom electrodes 11 set on the cathode substrate 10 are connected to a data line driver circuit 40 with an FPC 70, and the top electrode bus lines 16 are connected to a scan line driver circuit 50 with the FPC 70. In the data line driver circuit 40, data driver circuits D corresponding to the respective data lines 11 are arranged. In the scan line driver circuit 50, scan driver circuits S corresponding to the respective scan lines 16 are arranged.  
15

20 The spacer lines 16' are connected to the scan data driver circuit 50 through the FPC 70, and ground voltage is given thereto inside the driver circuit.

An excellent point of this manner is that ground voltage is given to the spacers 30 through the  
25 spacer lines 16' at the same time of the connection of the scan lines 16.

The pixel positioned at the intersection point of the <sup>m</sup>th top electrode bus line (scan line) 16 and

the  $n$ th bottom electrode (data line) 11 is represented by the coordinate (m, n). A high voltage of about 1 to 10 kV is applied to the metal back 114 from the high-voltage generating circuit 60.

5 As illustrated in FIG. 32, in the present example, it is supposed that the scan lines 16 and the data lines 11 are driven from one side of the cathode substrate 10. However, to arrange driver circuits on both sides thereof as the need arises does not prohibit 10 the present invention from being realized.

FIG. 33 illustrates an example of generated voltage waveforms in the respective driver circuits.

At time  $t_0$ , voltages at all of the electrodes are zero; therefore, no electrons are emitted so that 15 the phosphors do not emit any light.

At time  $t_1$ , voltage  $V_1$  is applied to only  $S_1$  out of the top electrode bus lines 16, and voltage  $-V$  is applied to  $D_2$  and  $D_3$  out of the bottom electrode lines 11. In the coordinates (1, 2) and (1, 3), 20 voltage  $(V_1+V_2)$  is applied between the bottom electrode 11 and the top electrode bus line 16. For this reason, when voltage  $(V_1+V_2)$  is set to a value not less than 25 electron emitting start voltage, electrons are emitted from these MIM type electron sources to vacuum. The emitted electrons are accelerated by the high voltage applied to the metal back 114 from the high-voltage generating circuit 60, and then radiated into the phosphors, so that light is emitted.

In the case that voltage V1 is applied to S2 out of the top electrode bus lines 16 and voltage -V2 is applied to D3 out of the bottom electrodes 11 similarly at time t2, the coordinate (2, 3) is switched 5 on in the same manner so as to emit electrons. As a result, the phosphor on this electron source coordinate emits light.

As described above, desired images or data can be displayed by changing scan signals applied to the 10 top electrode bus lines 16. Images having a gray scale can be displayed by changing the value of voltage -V2 applied to the bottom electrodes 11 appropriately.

At time t5, a reverse bias is applied in order to release charges accumulating in the tunneling 15 insulator 12. In other words, voltage -V3 is applied to all of the top electrode bus lines 16 and simultaneously 0 V is applied to all of the bottom electrodes 11.

In the present example, the voltage at the scan 20 lines which are not selected is set to 0 V (ground voltage). However, as described in Patent Document 3 (Japanese Patent Application laid-Open No. 2001-83907), the use of the manner of cutting down reactive current, which follows charge-discharge, by keeping the non- 25 selected scan lines in a high impedance state does not prohibit the present invention from being realized.

#### Example 2

This example discloses a manner that ground

voltage is applied to the spacer lines 16' without being passed through the scan line driver circuit 50. First, according to Example 1, the cathode substrate 10 comprising MIM electron sources, the anode substrate 5 110 and the panel 120 are formed.

FIG. 34 is a connection diagram illustrating the display device panel 120, which is formed as described above, connected to driver circuits. The bottom electrodes 11 are connected to the data line 10 driver circuit 40 through the FPC 70, and the top electrode bus lines 16 are connected to the scan line driver circuit 50 through the FPC 70.

In the same way, the spacer lines 16' are connected to the scan line driver circuit 50 through the FPC 70. The FPC 70 used herein is made up to a circuit having internal lines for short-circuiting all of the spacer lines 16' in advance. In a terminal portion of the FPC 70, the unified spacer lines are connected to a ground line independently of the scan 20 line driver circuit 50.

An excellent point of this manner is that even if arc discharge is generated inside the panel 120 to apply a high voltage to the spacer lines 16', the effect thereof is not produced on the scan line driver 25 circuit 50.

### Example 3

This example discloses another manner that ground voltage is applied to the spacer lines 16'

without being passed through the scan line driver circuit 50. First, according to Example 1, the cathode substrate 10 comprising MIM electron sources, the anode substrate 110 and the panel 120 are formed.

5 In this case, attention should be paid to the matter that in the cathode substrate 10 terminals of the spacer lines 16' are extended to the outside of the top electrode bus lines 16 so as to be mutually short-circuited, which is different from Example 2.

10 FIG. 35 is a connection diagram illustrating the display device panel, which is formed as described above, connected to driver circuits. The bottom electrodes 11 are connected to the data line driver circuit 40 through the FPC 70, and the top electrode bus lines 16 are connected to the scan line driver circuit 50 through the FPC 70. The spacer lines 16' are unified at one end of the cathode substrate and on the cathode substrate, so as to be connected to independent ground lines.

15 20 An excellent point of this manner is that ground lines having a low impedance can be introduced without limitation based on the performance of the FPC 70. Consequently, even if arc discharge is generated inside the panel to apply a high voltage to the spacer lines 16', damage to the scan line driver circuit 50 can be completely avoided.

#### Example 4

An example according to the second aspect of

the present invention will be described with reference to FIGS. 17 to 45.

(1) Formation of a cathode substrate 10:

This item describes a production process in a case in which top electrodes 13 are connected electrically to an underlying layer 15A and further top electrode bus lines 16 are backed with aluminum, aluminum alloy, or a metal having a lower resistivity than aluminum.

It is beforehand stated that the MIM electron source producing process which can be used in the present invention is not limited to the present example. The present invention can easily be applied to MIM electron sources disclosed in Patent Documents 1 and 2 (Japanese Patent Application Laid-Open Nos. 2001-101965 and 2000-208076), which comprise top electrode bus lines having a tapered structure, and other MIM electron sources.

Electron sources are produced in accordance with the manner described in Example 1, as shown in FIGS. 3 to 8. The finished electron sources are illustrated in FIG. 36 (a plan view), FIG. 37 (a sectional view taken on line A-A'), and FIG. 38 (a sectional view taken on line B-B'). The electrical lines 16 and 16' positioned, as the upper layer, inside each of sub-pixels in Example 1 and illustrated in FIGS. 21, 22 and 23 are converted to one scan line 16 in this example and the width thereof is made two times wider

so as to make the impedance thereof lower. In short, this example is characterized in that the spacer lines 16' and the scan lines 16 are made common.

Consequently, the step of forming the top electrodes 16  
5 is also made simpler than that in Example 1.

The reason why some parts of the scan lines 16 can be used both as the spacer lines 16' and scan lines without dividing the top electrode bus lines into the scan lines 16 and the spacer lines 16' by etching will  
10 be briefly described hereinafter.

The voltage applied to the scan lines 16 is usually as low as about 5 V, but the voltage applied to the metal back 14 of the finished anode substrate 110 (i.e., the acceleration voltage) is as high as 1 to 10  
15 kV as described above. From this fact, the voltage applied to the scan lines 16 can be substantially regarded as ground voltage, as compared with the high voltage (acceleration voltage) applied to the metal back 114. In short, the scan lines can be regarded as  
20 spacer ground lines. Consequently, some parts of the scan lines 16 can be used both as the spacer lines 16' and scan lines without making the spacer lines independent.

The finished cathode substrate 10 wherein  
25 electron sources are arranged is schematically illustrated in FIG. 39 (a plan view), FIG. 40 (a sectional view taken on line A-A'), and FIG. 41 (a sectional view taken on line B-B'). To simplify the

description hereinafter, the finished substrate 10 which is a 3 × 4 dot MIM type electron source substrate is illustrated. In any actual display panel, an MIM type electron source matrix wherein the number of MIM 5 type electron sources corresponds to the number of display dots should be formed.

In the case that a display device is constructed, electrode ends of the bottom electrodes 11 and the top electrode bus lines 16 must be made naked 10 in order to connect the ends to driver circuits although this matter has not been referred to, in the description on the process for producing the MIM type electron source, hereinbefore.

(2) Formation of the anode substrate 110:

15 The anode substrate 110 wherein a phosphor surface is formed is formed in the manner as disclosed in Example 1.

(3) Formation of a display panel:

Sections of the display panel 120 in the state 20 that the finished anode substrate 110 and the above-mentioned cathode substrate 10 are adhered to each other are illustrated in FIG. 42 (a sectional view taken on line A-A') and 43 (a sectional view taken on line B-B'). These sectional views taken on line A-A' 25 and line B-B correspond to line A-A' and line B-B' in cases where the cathode substrate 10 and the anode substrate 110 are drawn, respectively.

The spacers 30 are connected to some parts of

the upper portions of the scan lines 16 (so as to avoid the electron emission area).

FIG. 44 schematically illustrates the state that this display panel 120 is connected to driver circuits. As described above, the lower ends of the spacers 30 are connected to the scan lines 16, and the scan lines 16 are connected to the scan line driver circuit 50 through the FPC 70.

FIG. 45 shows driving voltage waveforms when the display panel 120 produced in the present example is connected to the driver circuits as illustrated in FIG. 44 and driven. Basically, this figure is the same as FIG. 33 illustrating Example 1. In the present example, however, there are no independent spacer lines 16', and at the time of selecting a given scan line out of the scan lines 16 (selecting the electron source at a given coordinate), scan line voltage V1 is applied through the scan line beneath the lower end of the spacer. This point is different from Example 1.

Needless to say, when the electron source at a given coordinate is selected by selecting a given line out of the scan lines, electrons are emitted from the electron emission area of this selected electron source. As a result, the spacers adjacent to the electron source are charged up. Thus, in the present example, the voltage of the spacers 30 is fixed to a lower voltage (scan line voltage) than the anode voltage (the acceleration voltage applied to the metal back 114 of

the anode substrate 110) at the least in the period when the electrons are emitted, whereby the electrification of the spacers can be removed by the surface conduction of the spacers. It is important for 5 suppressing distortion of the orbit of the electrons or creeping discharge to prevent the electrification of the spacers 30.

In the case of the present example, the scan line voltage is as low as about 5 V while the anode 10 voltage is as high as about 1 to 10 kV. Therefore, the voltage of the spacer 30 connected to this scan line substantially becomes ground voltage, so that the electrification can be sufficiently prevented.

When this scan line is not selected, reactive 15 current following charge-discharge can be cut off by keeping the scan line, the voltage of which is usually fixed to 0 V, in a high impedance state, as described in Patent Document 3 (Japanese Patent Application Laid-Open No. 2001-83907). The use of this manner does not 20 prohibit the present invention from being realized.

As described above, the desired objects can be attained by the present invention. In other words, in the step of producing a cathode substrate having two-layer lines, the second lines are caused to function 25 both as scan lines and spacer (ground) lines, whereby ground lines for the spacers can be set up without increasing the number of lines. As a result, the production process can be shortened and a high yield

can be attained so that costs can be reduced.